IN THE CLAIMS

1. (Previously Presented) A method of providing access to a bus, comprising:

receiving a plurality of device access requests for the bus, each of the plurality of device access requests being received from one of a plurality of processing devices not connected to the bus, each of the plurality of processing devices having a switch associated therewith;

selecting a particular one of the plurality of device access requests according to a predetermined priority protocol;

generating a control signal corresponding to the selected particular one of the plurality of device access requests;

providing the control signal to a particular one of the plurality of processing devices that sent the selected particular one of the plurality of device access requests, the control signal enabling the switch associated with the particular one of the plurality of processing devices to connect the particular one of the plurality of processing devices to the bus;

selecting a next one of the plurality of device access requests according to the predetermined priority protocol;

generating a control signal corresponding to the selected next one of the plurality of device access requests;

providing the control signal to a next one of the plurality of processing devices that sent the selected next one of the plurality of device access requests, the control signal enabling the switch associated with the next one of the plurality of processing devices to connect the next one of the plurality of processing devices to the bus prior to an end of the particular one of the plurality of processing devices being connected to the bus, the remaining ones of the

plurality of processing devices not being connected to the bus in order to minimize a load on the bus.

2. (Original) The method of Claim 1, wherein the bus is a PCI bus.

3. (Original) The method of Claim 2, wherein the PCI bus operates at a frequency of at least 66 MHz.

4. (Previously Presented) The method of Claim 1, wherein the plurality of device access requests are received from processing devices desiring to communicate over the bus.

5. (Canceled).

6. (Canceled).

7. (Previously Presented) The method of Claim 1, further comprising:

determining an end for the particular one of the plurality of processing devices to be connected to the bus;

initiating access of the next one of the plurality of processing devices to the bus in response to the end for the particular one of the plurality of processing devices to be connected to the bus.

8. (Previously Presented) The method of Claim 7, further comprising:

generating a disabling control signal in response to the end for the particular one of the plurality of processing devices to be connected to the bus;

disconnecting the particular one of the plurality of processing devices from the bus in response to the disabling control signal.

9. (Original) The method of Claim 1, further comprising:

limiting a number of generated control signals in order to control a load on the bus.

10. (Previously Presented) The method of Claim 1, further comprising:

generating a disable control signal for a request not selected in order to prevent connecting of an associated processing device to the bus.

11. (Previously Presented) A system for providing access to a bus, comprising:

a bus controller;

a plurality of processing devices capable of being connected to the bus controller by a bus;

a plurality of enabling switches on the bus, each enabling switch connected to a corresponding processing device, each enabling switch determining whether the corresponding processing device is connected to the bus in response to a control signal from the bus controller;

wherein the bus control receives a plurality of requests from the plurality of processing devices, the bus controller operable to select a highest priority request, the bus controller operable to generate a first control signal for a first enabling switch associated with a first processing device having the highest priority request, the first enabling switch connecting the first processing device to the bus for access thereto;

wherein the bus controller is operable to select a next highest priority request, the bus controller operable to generate a second control signal for a second enabling switch associated with a second processing device having the next highest priority request, the second enabling switch connecting the second processing device to the bus, the bus controller allowing the second processing device to be connected to the bus prior to disconnecting the first processing device from the bus, wherein remaining ones of the plurality of processing devices are not connected to the bus in order to minimize a load on the bus.

12. (Previously Presented) The system of Claim 11, wherein the bus controller allows simultaneous connecting to the bus by a predetermined number of the plurality of processing devices in order to limit a load on the bus.

13. (Previously Presented) The system of Claim 11, wherein the bus controller receives a plurality of device access requests from the plurality of processing devices for connecting to the bus.

14. (Previously Presented) The system of Claim 13, wherein the bus controller arbitrates the plurality of device access requests from the plurality of processing devices according to a predetermined protocol.

15. (Original) The system of Claim 11, wherein the bus is a PCI bus.

16. (Original) The system of Claim 15, wherein the PCI bus operates at a frequency of approximately 66 MHz.

17. (Previously Presented) A PCI bus, comprising:

a plurality of pass transistors, each pass transistor operable to provide connecting of an associated processing device to the bus, each pass transistor operable to receive a control signal to connect and disconnect its associated processing device to and from the bus, wherein a first pass transistor connects a first processing device to the bus for access thereto in response to a first control signal, a second pass transistor connects a second processing device to the bus in response to a second control signal prior to disconnecting of the first processing device from the bus upon an end of access thereto, wherein the remaining ones of the plurality of pass transistors do not connect their respective processing devices to the bus when the first processing device and the second processing device are connected to the bus.

18. (Original) The PCI bus of Claim 17, wherein a particular pass transistor receives an enable control signal in response to an access request sent by its associated processing device.

19. (Previously Presented) The PCI bus of Claim 17, wherein a particular pass transistor is operable to disconnect its associated processing device from the bus such that the particular processing device does not appear to be connected to the PCI bus in order to reduce a load on the bus.

20. (Original) The PCI bus of Claim 17, wherein each of the processing devices is operable to communicate at a 66 MHz rate.